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09/773,543	02/02/2001	Shunpei Yamazaki	12732-012001 / US4638	8040

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EXAMINER	
MANDALA, VICTOR A	
ART UNIT	**PAPER NUMBER**
2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/773,543	Applicant(s) YAMAZAKI ET AL.	
	Examiner Victor A Mandala Jr.	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 February 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5, 6, 10* .
4) ☐ Interview Summary (PTO-413) Paper No(s).
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

6,8,10

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Species II Figure 5 in Paper No. 13 is acknowledged. Claims 1-37 will be examined.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the connection electrode and or source wiring must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-37 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,303,963 Ohtani et al.

The applied reference has common inventors with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

3. Referring to claim 1, a semiconductor device comprising: a semiconductor layer, (Figure 8 #s 805, 802, 803, & 805), formed on an insulating surface, (Figure 8 #801), and having at least a source region, (Figure 8 examiner's label #866), a drain region, (Figure 8 # 803 & 804), and a channel formation region, (Figure 8 #802), interposed there-between; a first insulating film, (Figure 8 #807), formed on said semiconductor layer, (Figure 8 #s 805, 802, 803, & 805); at least one electrode, (Figure 8 #808), formed on said first insulating film, (Figure 8 #807), and overlapping said channel formation region, (Figure 8 #802); a source wiring, (Figure 8 #816), formed on said first insulating film, (Figure 8 #807); a second insulating film, (Figure 8 #820), covering at least said at least one electrode, (Figure 8 #808), and said source wiring, (Figure 8 #816), and a gate wiring, (Figure 9 #902), formed on said second insulating film, (Figure 8 #820), and connected to said at least one electrode, (Figure 8 #808).

4. Referring to claim 2, a semiconductor device, wherein said gate wiring, (Figure 9 #902), overlaps a portion of said semiconductor layer, (Figure 8 #s 805, 802, 803, & 805), containing at least said channel formation region, (Figure 8 #802).

5. Referring to claim 3, a semiconductor device, wherein said at least one electrode, (Figure 8 #808), comprises a gate electrode, (Figure 8 #808).

6. Referring to claim 4, a semiconductor device, wherein said at least one electrode, (Figure 8 #808), and said source wiring, (Figure 8 #816), comprise a same material, (Col. 8 Lines 59-63 & Col. 19 Lines 24-35).

7. Referring to claim 5, a semiconductor device, wherein a material of said gate wiring, (Figure 9 #902), comprises one or a plurality of elements selected from the group consisting of polySi, W, WSi, At, Cu, Ta, Cr and Mo, (Col. 19 Lines 24-35).

8. Referring to claim 6, a semiconductor device, wherein said first insulating film, (Figure 8 #807), comprises a gate insulating film, (Figure 8 #807).

9. Referring to claim 7, a semiconductor device, wherein said second insulating film, (Figure 8 #820), further comprises a first insulating layer, (Figure 8 #807), containing silicon as a main component and a second insulating layer, (Figure 8 #820), containing an organic resin material, (Col. 8 Lines 46-67).

10. Referring to claim 8, a semiconductor device, wherein said group consisting of a personal computer, a semiconductor device is one selected from the video camera, a portable information terminal, a digital camera, a digital video disk player, a portable telephone, an electronic book, a projector, a head mounted type display, and an electric game appliance, (Figures 11 & 22).

11. Referring to claim 9, a semiconductor device comprising: a semiconductor layer, (Figure 8 #s 802 & 803), formed on an insulating surface, (Figure 8 # 801), and having at least a source region, (Figure 8 examiner's label #866), a drain region, (Figure 8 # 803 & 804), and a channel formation region, (Figure 8 #802), inter-posed there-between; a first insulating, (Figure 8 #807), formed on said semiconductor layer, (Figure 8 #s 802 & 803): at least one electrode, (Figure 8 #808), formed on said first insulating film, (Figure 8 #807), and overlapping said channel formation region; a source wiring, (Figure 8 #805), formed on said first insulating film, (Figure 8 #807); a second insulating film, (Figure 8 #820), covering at least said at least one electrode, (Figure 8 #808), and said source wiring, (Figure 8 #805), a gate wiring, (Figure 9 #902), formed on said second insulating film, (Figure 8 #820), and connected to said at least one electrode, (Figure 8 #808); a connection electrode, (Figure 8 #816), formed on said second insulating film, (Figure 8 # 820), and connected to said source wiring, (Figure 8 #805), and said semiconductor layer, (Figure 8 #s 802 & 803); and a pixel electrode, (Figure 18 #3609), formed on said second insulating film, (Figure 8 # 820), and electrically connected to said semiconductor layer, (Figure 8 #s 802 & 803).

12. Referring to claim 10, a semiconductor device, wherein said pixel electrode, (Figure 18 #3609), overlaps said source wiring, (Figure 18 examiner's label #1z).

13. Referring to claim 11, a semiconductor device, wherein said gate wiring, (Figure 9 #902), overlaps a portion of said semiconductor layer, (Figure 8 #s 802 & 803), containing at least said channel formation region, (Figure 8 # 802).

14. Referring to claim 12, a semiconductor device, wherein said at least one electrode comprises a gate electrode, (Figure 8 #808).

15. Referring to claim 13, a semiconductor device, wherein said at least one electrode, (Figure 8 #808), and said source wiring, (Figure 8 #816), comprise a same material, (Col. 8 Lines 59-63 & Col. 19 Lines 24-35).

16. Referring to claim 14, a semiconductor device, wherein said pixel electrode, said connection electrode and said gate wiring comprise the same material, (Col. 8 Lines 59-63 & Col. 19 Lines 24-35).

17. Referring to claim 15, a semiconductor device, wherein a material of said gate wiring comprises one or a plurality of elements selected from the group consisting of polySi, W, WSix, Al, Cu, Ta, Cr and Mo, (Col. 19 Lines 24-35).

18. Referring to claim 16, a semiconductor device, wherein said first insulating film comprises a gate insulating film, (Figure 8 #802).

19. Referring to claim 17, a semiconductor device, wherein said second insulating film, (Figure 8 #820), further comprises a first insulating layer, (Figure 8 #807), containing silicon as a main component and a second insulating layer, (Figure 8 #820), containing an organic resin material, (Col. 8 Lines 46-67).

20. Referring to claim 18, a semiconductor device, wherein one pixel including said pixel electrode, (Figure 20 #3616), forms a storage capacitor, (Figure 20 capacitor involves 3616 and dielectric 3608 & 3607 between semiconductor layer, examiner's label, #7777), between said semiconductor layer, (Figure 20 Examiner's label #7777), connected to said pixel electrode, (Figure 20 #3616), and said at least one electrode, (Figure 8 #808), connected to a gate wiring, (Figure 9 #902), of an adjacent pixel, using said first insulating film, (Figure 8 #807), as a dielectric.

21. Referring to claim 19, a semiconductor device, wherein an impurity element for imparting a p-type conductivity is added to said semiconductor layer, (Figure 20 TFT #3503 Col. 27 Line 29), connected to said pixel electrode, (Figure 20 # 3616).

22. Referring to claim 20, a semiconductor device, said semiconductor device is one selected from the group consisting of a personal computer, a video camera, a portable information terminal, a digital camera, a digital video disk player, a portable telephone, an electronic book, a projector, a head mounted type display, and an electric game appliance, (Figures 11 & 22).

23. Referring to claim 21, a semiconductor device comprising: a first insulating film, (Figure 8 #807), adjacent to a semiconductor layer, (Figure 8 #s 805, 802, 803, & 805), said semiconductor layer, (Figure 8 #s 805, 802, 803, & 805), having at least a source region, (Figure 8 examiner's label #866), a drain region, (Figure 8 # 803 & 804), and a channel formation region, (Figure 8 #802), interposed there-between; at least one electrode, (Figure 8 #808), including a gate electrode, (Figure 8 #808), formed on said first insulating film, (Figure 8 #807); a source wiring, (Figure 8 #816), formed on said first insulating film, (Figure 8 #807); a second insulating film covering at least said at least one electrode, (Figure 8 #808), and said source wiring; a gate wiring, (Figure 9 #902), electrically connected to said at least one electrode, (Figure 8 #808); and a pixel electrode, (Figure 20 # 3616), electrically connected to said semiconductor layer, (Figure 20 Examiner's label #7777), wherein said gate wiring, (Figure 9 #902), and said pixel electrode, (Figure 20 # 3616), are formed on said second insulating film, (Figure 20 #3608).

24. Referring to claim 22, a semiconductor device, wherein said gate wiring, (Figure 9 #902), overlaps a portion of said semiconductor layer, (Figure 8 #s 805, 802, 803, & 805), containing at least said channel formation region, (Figure 8 #802).

25. Referring to claim 23, a semiconductor device, wherein said at least one electrode, (Figure 8 #808), and said source wiring, (Figure 8 #816), comprise a same material, (Col. 8 Lines 59-63 & Col. 19 Lines 24-35).

26. Referring to claim 24, a semiconductor device, wherein a material of said gate wiring comprises one or a plurality of elements selected from the group consisting of polySi, W, WSi, Al, Cu, Ta, Cr and Mo, (Col. 19 Lines 24-35).

27. Referring to claim 25, a semiconductor device, wherein said first insulating film, (Figure 8 #807), comprises a gate insulating film, (Figure 8 #807).

28. Referring to claim 26, a semiconductor device, wherein said second insulating film, (Figure 8 #820), further comprises a first insulating layer, (Figure 8 #807), containing silicon as a main component and a second insulating layer, (Figure 8 #820), containing an organic resin material, (Col. 8 Lines 46-67).

29. Referring to claim 27, a semiconductor device, wherein said semiconductor device is one selected from the group consisting of a personal computer, a video camera, a portable information terminal, a digital camera, a digital video disk player, a portable telephone, an electronic book, a projector, a head mounted type display, and an electric game appliance, (Figures 11 & 22).

30. Referring to claim 28, a semiconductor device comprising a pair of substrates, (Figure 4 #10 & 66), and a liquid crystal interposed, (Figure 4 #69), there-between, one of said pair of

substrates, (Figure 4 #10 & 66), having at least a pixel portion, (Figure 4 Pixel Matrix Portion), and a driver circuit, (Figure 4 Peripheral Circuit), said pixel portion, (Figure 4 Pixel Matrix Portion), comprising: a semiconductor layer, (Figure 8 #s 805, 802, 803, & 805), formed on an insulating surface, (Figure 8 #801), and having at least a source region, (Figure 8 examiner's label #866), a drain region, (Figure 8 # 803 & 804), and a channel formation region, (Figure 8 #802), interposed there-between; a first insulating film, (Figure 8 #807), formed on said semiconductor layer, (Figure 8 #s 802 & 803), at least one electrode, (Figure 8 #808), formed on said first insulating film, (Figure 8 #807), and overlapping at least said channel formation region, (Figure 8 #802); a source wiring, (Figure 8 #805), formed on said first insulating film, (Figure 8 #807); a second insulating film, (Figure 8 #820), covering at least said at least one electrode, (Figure 8 #808), and said source wiring, (Figure 8 #805); a gate wiring, (Figure 8 #808), formed on said second insulating film, (Figure 8 #820), and connected to said at least one electrode, (Figure 8 #808); a connection electrode, (Figure 8 #816), formed on said second insulating film, (Figure 8 #820), and connected to said source wiring, (Figure 8 #805), and said semiconductor layer, (Figure 8 #s 802 & 803); and a pixel electrode, (Figure 20 # 3616), formed on said second insulating film, (Figure 20 #3608), and electrically connected to said semiconductor layer, (Figure 20 Examiner's label #7777), and wherein another one of said pair of substrates, (Figure 4 #10 & 66), comprises a light-shielding film in which a red color filter and a blue color filter, (Col. 14 Lines 60-62 & Col. 28 Lines 25-28), are laminated so as to overlap said semiconductor layer, (Figure 8 #s 805, 802, 803, & 805).

31. Referring to claim 29, a semiconductor device, further comprising a common wiring, (Figure 20 #3620), on said second insulating film, (Figure 20 #3608), wherein said pixel electrode, (Figure 20 #3616), and said common wiring, (Figure 20 #3620), are arranged so that an electric field substantially parallel to a surface of said substrate, (Figure 20 #3501), is generated.

32. Referring to claim 30, a semiconductor device, said semiconductor device is a reflection-type liquid crystal display device in which said pixel electrode comprises a film containing Al or Ag or a lamination film thereof, (Col. 28 Lines 12-19).

33. Referring to claim 31, a semiconductor device, said semiconductor device is a transmission-type liquid crystal display device in which said pixel electrode comprises a transparent electrically conductive film, (Col. 29 Lines 60-61).

34. Referring to claim 32, a semiconductor device, said semiconductor device is one selected from the group consisting of a personal computer, a video camera, a portable information terminal, a digital camera, a digital video disk player, a portable telephone, an electronic book, a projector, a head mounted type display, and an electric game appliance, (Figures 11 & 22).

35. Referring to claim 33, a semiconductor device comprising a pair of , (Figure 4 #10 & 66), and a liquid crystal interposed, (Figure 4 #69), there-between, one of said pair of substrates, (Figure 4 #10 & 66), having at least a pixel portion, (Figure 4 Pixel Matrix Portion), and a driver circuit, (Figure 4 Peripheral Circuit), said pixel portion, (Figure 4 Pixel Matrix Portion), comprising: a semiconductor layer, (Figure 8 #s 805, 802, 803, & 805), formed on an insulating surface, (Figure 8 #801), and having at least a source region, (Figure 8 examiner's label #866), a drain region, (Figure 8 # 803 & 804), and a channel formation region, (Figure 8 #802),

interposed there-between; a first insulating film, (Figure 8 #807), formed on said semiconductor layer, (Figure 8 #s 802 & 803), at least one electrode, (Figure 8 #808), formed on said first insulating film, (Figure 8 #807), and overlapping at least said channel formation region, (Figure 8 #802); a source wiring, (Figure 8 #805), formed on said first insulating film, (Figure 8 #807); a second insulating film, (Figure 8 #820), covering at least said at least one electrode, (Figure 8 #808), and said source wiring, (Figure 8 #805); a gate wiring, (Figure 8 #808), formed on said second insulating film, (Figure 8 #820), and connected to said at least one electrode, (Figure 8 #808); and a pixel electrode, (Figure 20 # 3616), formed on said second insulating film, (Figure 20 #3608), and electrically connected to said semiconductor layer, (Figure 20 Examiner's label #7777).

36. Referring to claim 34, a semiconductor device, further comprising a common wiring, (Figure 20 #3620), on said second insulating film, (Figure 20 #3608), wherein said pixel electrode, (Figure 20 #3616), and said common wiring, (Figure 20 #3620), are arranged so that an electric field substantially parallel to a surface of said substrate, (Figure 20 #3501), is generated.

37. Referring to claim 35, a semiconductor device, said semiconductor device is a reflection-type liquid crystal display device in which said pixel electrode comprises a film containing Al or Ag or a lamination film thereof, (Col. 28 Lines 12-19).

38. Referring to claim 36, a semiconductor device, said semiconductor device is a transmission-type liquid crystal display device in which said pixel electrode comprises a transparent electrically conductive film, (Col. 29 Lines 60-61).

39. Referring to claim 37, a semiconductor device, said semiconductor device is one selected from the group consisting of a personal computer, a video camera, a portable information terminal, a digital camera, a digital video disk player, a portable telephone, an electronic book, a projector, a head mounted type display, and an electric game appliance, (Figures 11 & 22).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A Mandala Jr. whose telephone number is (703) 308-6560. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

VAMJ
February 22, 2003